AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions of the claims and any prior listing of the claims in the present application. The status of each claim is shown in parentheses.

In the following listing, Claims 8, 18–21 and 23 are cancelled herein. Claims 1, 12, 22 and 24–29 are currently amended. Claims 2–7, 9–11 and 13-21 remain as originally filed.

Listing of Claims

Claim 1 **(Currently Amended)**: A buffer memory controller for a hard disk controller, the buffer memory controller comprising:

a data buffer configured to buffer write operation data between a buffer memory and a write head of a disk;

a plurality of address registers configured to store, for each of a plurality of write operations, an address identifying a location of corresponding write operation data stored within the buffer memory; and

controller logic configured to transfer, for each of the write operations, the corresponding write operation data from the buffer memory to the data buffer based at least upon the corresponding address stored in the address registers, wherein the controller logic is further configured to transfer, based upon a single command to the controller logic, the data of at least two write operations in an order other than the order in which the at least two write operations were received in the buffer memory.

Claim 2 **(Original)**: The buffer memory controller of Claim 1, further comprising a plurality of block count registers configured to store, for each of the write operations, the corresponding amount of write operation data stored within the buffer memory.

Claim 3 **(Original)**: The buffer memory controller of Claim 2, wherein the controller logic is further configured to perform the transfers based additionally upon the quantities stored in the block count registers.

Claim 4 **(Original)**: The buffer memory controller of Claim 3, wherein the block count registers operate as a FIFO.

Claim 5 **(Original)**: The buffer memory controller of Claim 1, wherein the data buffer operates as a FIFO.

Claim 6 **(Original)**: The buffer memory controller of Claim 1, wherein the data buffer is configured to supply write operation data to a disk formatter.

Claim 7 **(Original)**: The buffer memory controller of Claim 1, wherein the address registers operate as a FIFO.

Claim 8 **(Cancelled)**

Claim 9 **(Original)**: The buffer memory controller of Claim 1, further comprising a busy flag configured to indicate whether the address registers are full.

Claim 10 **(Original)**: The buffer memory controller of Claim 1, wherein the number of address registers is at least 4.

Claim 11 **(Original)**: The buffer memory controller of Claim 1, wherein the number of address registers is at least 8.

Claim 12 **(Currently Amended)**: A method of operating a hard disk unit, the method comprising:

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(A) receiving a first write operation;

(B) subsequent to (A), receiving a second write operation;

4 (C) receiving a single command from a processor to provide the data from the first write operation and the data from the second write operation to a disk formatter;

([[C]] D) writing the data of the second write operation to a disk; and

([[D]] E) subsequent to ([[C]] D), writing the data of the first write operation to the disk.

Claim 13 (Original): The method of Claim 12, further comprising determining that the first write operation and the second write operation write data to the same track.

Claim 14 **(Original)**: The method of Claim 13, further comprising determining that the second write operation has a lower ending sector number than the starting sector number of the first write operation.

Claim 15 **(Original)**: The method of Claim 13, further comprising determining that the second write operation is located before the first write operation relative to the position where the write head of the disk is capable of first writing to the track.

Claim 16 **(Original)**: The method of Claim 13, wherein a portion of the data of the first write operation and a portion of the data of the second write operation are written to the disk during a single revolution.

Claim 17 **(Original)**: The method of Claim 13, wherein the data of the first write operation and the data of the second write operation are completely written to the disk unit during a single revolution.

Claims 18–21 **(Cancelled)**

Claim 22 **(Currently Amended)**: A method of operating a hard disk controller, the A3 method comprising:

receiving a first write operation;

receiving a second write operation subsequent to receiving the first write operation;

loading a first address register of a buffer memory controller with an address in a buffer memory of write operation data of ~~a first~~ the second write operation; [[and]]

loading a second address register of the buffer memory controller with an address in the buffer memory of write operation data of ~~a second~~ the first write operation, wherein the first address register is different then than the second address register and wherein the first write operation is different than the second write operation;

receiving a single command from a processor to provide both the data of the first write operation and the data of the second write operation to a disk formatter; and

writing the data of the second write operation prior to writing the data of the first write operation.

Claim 23 **(Cancelled)**

Claim 24 **(Currently Amended)**: A method of operating a buffer memory controller of a hard disk controller, the method comprising:

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(A) for each of a plurality of write operations, receiving in a different one of a plurality of address registers of the buffer memory controller, an address, within a buffer memory, of write operation data of the respective write operation; ~~and~~

(B) receiving a single command to provide the write operation data of the plurality of write operations; and

(C) writing the data of the plurality of write operations in an order other than the order in which the data of each of plurality of write operations was received by the buffer memory.

Claim 25 **(Currently Amended)**: The method of Claim 24, further comprising[[,]]:

([[C]] D) for each of the write operations, receiving in a different one of a plurality of block count registers of the buffer memory controller, a value specifying an amount of write operation data associated with the respective write operation.

Claim 26 **(Currently Amended)**: The method of Claim 25, further comprising[[,]]:

([[D]] E) for one of the write operations, transferring write operation data from the buffer memory, the amount of which write operation data is specified by the value in the corresponding block count register and the address of which write operation data is specified by the address in corresponding address register.

Claim 27 **(Currently Amended)**: The method of Claim 26, further comprising, on the buffer memory controller, repeating ([[D]] E) for each of the remaining write operations.

Claim 28 **(Currently Amended)**: A disk drive controller comprising:

~~a microprocessor;~~

a buffer memory for storing write operation data;

a buffer memory controller, the buffer memory controller comprising:

a data buffer configured to buffer write operation data between the buffer memory and a write head of a disk;

a plurality of address registers configured to store, for each of a plurality of write operations, an address identifying a location of corresponding write operation data stored within the buffer memory; and

controller logic configured to transfer, for each of the write operations, the corresponding write operation data from the buffer memory to the data buffer based at least upon the corresponding address stored in the address registers;

and

~~firmware code that is executed by the~~ a microprocessor that issues commands to the controller logic, the ~~firmware code~~ microprocessor configured to ~~enable the microprocessor~~ perform write operations based upon the buffered write operation data in an order other than the order in which the write operations are received by the ~~controller~~ buffer memory.

Claim 29 **(Currently Amended)**: ~~The disk drive controller of Claim 28,~~ A disk drive controller comprising:

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a buffer memory for storing write operation data;

a buffer memory controller comprising:

a data buffer configured to buffer write operation data between the buffer memory and a write head of a disk;

a plurality of address registers configured to store, for each of a plurality of write operations, an address identifying a location of corresponding write operation data stored within the buffer memory; and

controller logic configured to transfer, for each of the write operations, the corresponding write operation data from the buffer memory to the data buffer based at least upon the corresponding address stored in the address registers;

and

a microprocessor that issues commands to the controller logic, the microprocessor configured to perform write operations in an order other than the order in which the write operations are received by the buffer memory, wherein the microprocessor executes firmware code ~~is configured to cause~~ that causes the microprocessor to:

(A) identify a first write operation received by the ~~controller~~ buffer memory;

(B) identify a second write operation received by the ~~controller~~ buffer memory after receiving the first write operation;

(C) load a first of the address registers of the buffer memory controller with an address in the buffer memory of the write operation data of the second write operation;

(D) load a second of the ~~of the~~ address registers of the buffer memory controller with an address in the buffer memory of the write operation data of the first write operation; and

(E) issue a single command to the buffer memory controller that causes the buffer memory controller to transfer the data identified by the first address register and to subsequently transfer the data identified by the second address register.